

DEPARTMENT OF  
ELECTRONICS & COMMUNICATION ENGINEERING

SCHEME OF COURSES FOR  
**M. Tech. (VLSI Design), Batch – 2020-2022**



**THAPAR INSTITUTE  
OF ENGINEERING & TECHNOLOGY  
(Deemed to be University)**

**SCHEME OF COURSES FOR  
M. Tech. (VLSI Design) – Batch: 2019 – 21**

**First Semester**

S. No.	Course Code	Course Name	L	T	P	Cr
1.	PVL108	Device Physics and Technology	3	1	0	3.5
2.	PVL204	FPGA Based System Design	3	0	2	4.0
3.	PVL103	Digital VLSI Design	3	1	2	4.5
4.	PVL206	Analog IC Design	3	1	2	4.5
5.	PVL203	VLSI Signal Processing	3	0	0	3.0
6.	PVL202	Embedded Systems	3	0	2	4.0
						23.5

**Second Semester**

S. No.	Course No.	Course Name	L	T	P	Cr
1.	PVL219	Physical Design Automation	3	1	0	3.5
2.	PVL208	VLSI Testing and Verification	3	0	2	4.0
3.	PVL220	CAD for VLSI Design	3	0	2	4.0
4.		Elective – I				4.0
5.		Elective – II				3.0
6.		Elective – III				3.0
	<b>Total</b>					21.5

**Third Semester**

S. No.	Course No.	Course Name	Cr
1.	PVL391	Seminar	4.0
2.	PVL***	Design Project	4.0
3.		Non-credit Self study online course (Swayam, MOOC, Coursera, NPTEL etc.)	Student must register the course with the consent of respective supervisor and also submit the passing certificate.
		<b>Dissertation (Starts)</b>	

**Fourth Semester**

S. No.	Course No.	Course Name	Cr
1.	PVL492	<b>Dissertation (Contd.....)</b>	<b>16.0</b>

**Total Credits – 69**

## List of Electives

<b>ELECTIVE – I</b>						
<b>S. No.</b>	<b>Course No.</b>	<b>Course Name</b>	<b>L</b>	<b>T</b>	<b>P</b>	<b>Cr</b>
1.	PVL224	MOS Device Modeling	3	0	2	4.0
2.	PVL207	Low Power System Design	3	0	2	4.0
3.	PVL230	System C	3	0	2	4.0
4.	PEC339	Image Processing and Computer Vision	3	0	2	4.0

<b>ELECTIVE – II</b>						
<b>S. No.</b>	<b>Course No.</b>	<b>Course Name</b>	<b>L</b>	<b>T</b>	<b>P</b>	<b>Cr</b>
1.	PVL332	Mixed Signal Circuit Design	3	0	0	3.0
2.	PVL331	Memory Design and Testing	3	0	0	3.0
3.	PVL110	VLSI Architectures	3	0	0	3.0
4.	PVL344	Hardware Algorithms for Computer Arithmetic	3	0	0	3.0
5.	PVL218	VLSI Interconnects	3	0	0	3.0
6.	PVL333	System on Chip	3	0	0	3.0
7.	PVL334	High Speed VLSI Design	3	0	0	3.0

<b>ELECTIVE – III</b>						
<b>S. No.</b>	<b>Course No.</b>	<b>Course Name</b>	<b>L</b>	<b>T</b>	<b>P</b>	<b>Cr</b>
1.	PVL216	VLSI Subsystem Design	3	0	0	3.0
2.	PVL335	Fault Tolerance in VLSI	3	0	0	3.0
3.	PVL343	Sensor Technology and MEMS	3	0	0	3.0
4.	PVL340	System Verilog	2	0	2	3.0
5.	PVL234	Machine Learning	3	0	0	3.0
6.	PVL235	RF IC Design	3	0	0	3.0
7.	PEC***	OPTOELECTRONICS DEVICES AND CIRCUITS	3	0	0	3.0

## PVL108: Device Physics and Technology

L T P  
3 1 0

**Course Objectives:** To understand the physics of semiconductor, basic theory of Metal Semiconductor Contacts and PN junction, construction and operation of semiconductor devices, operation and structure of MOS transistors, and basic theory of IC technology.

**Semiconductor Physics:** Semiconductor Materials, Crystal Structure, Energy Bands, Carrier Concentrations, Carrier Transport Phenomena, Continuity Equation, Thermionic Emission Process, Tunneling Process, High Field Effects.

**Semiconductor Devices:** p-n Junction, Thermal Equilibrium Condition, Depletion Region and Capacitance, IV and CV characteristics, Charge storage, Transient Behavior, Junction Breakdown, Metal Semiconductor Contacts, Tunnel diode- applications of tunnelling, Photonic Devices-LEDs, Semiconductor Laser, Photodiode, Bipolar Transistor, Thyristor, MOSFET Fundamentals and Scaling and MESFET.

**Semiconductor Technology:** Crystal Growth, Epitaxial- Growth Techniques, Structures and Defects, Film Formation, Deposition methods, Thermal Oxidation, Dielectric Deposition, Polysilicon and High-K dielectric, Lithography, Next Generation Lithographic Methods, Dry and Wet Chemical Etching, Impurity Doping, Diffusion-Related Processes, Implant-Related Processes, Annealing, Metallization, Integrated Devices, CMOS Fabrication Process, IC Packaging, Material and Device Characterization.

### Course Learning Outcomes:

On completion of this course, the students will be able to:

1. learn the basic physics of semiconductor.
2. understand the basic theory of semiconductor devices.
3. acquire the basics of crystal growth and its kinetics.
4. apply the semiconductor processing steps for device fabrication.

### Text Book:

1. *S. M Sze, VLSI Technology, 2<sup>nd</sup> Edition, Tata Mc Graw Hill, 2003.*
2. *BenG. Streetman, Solid State Electronic Devices, Prentice Hall*

### References:

1. *Yannis Tsividis, Operation and modeling of the MOS transistor, Mc Graw Hill, 1987.*
2. *S. M. Sze, Semiconductor Devices – Physics and Technology, 2<sup>nd</sup> Edition, Wiley, 2010.*

S.No.	Evaluation Elements	Weightage (%)
1.	MST	30
2.	EST	45
3.	Sessionals (May include Assignments/Projects/Tutorials/Quizes/Lab Evaluations)	25

## PVL109: FPGA based System Design

<b>L</b>	<b>T</b>	<b>P</b>
<b>3</b>	<b>0</b>	<b>2</b>

**Course Objectives:** In this course the students will learn logic synthesis with design optimization techniques, VHDL and Verilog design concepts, Combinational logic concepts, sequential VHDL processing and FPGA.

**Introduction:** Concepts of Hardware Description Languages,

**VHDL:** objects, types and subtypes, operators, packages

**Logic synthesis:** Design cycle, types of synthesizers, design optimization techniques, technology mapping, design organization.

**Combinational Logic:** Design units, entities and architectures, simulation and synthesis model, signals and ports, simple signal assignments, conditional signal assignments, selected signal assignment.

**Sequential logic design:** Processes, variables, sequential statements, Registers: Simulation and synthesis model of register, register templates, clock types, gated registers, resettable registers, simulation model of asynchronous reset, asynchronous reset templates, registered variables, FSM: Moore and Mealy machine modelling.

**Hierarchy:** components, component instances, component declaration, generate statements, Configuration specifications, default binding, binding process, component packages.

**Sub programs:** Functions, procedures, declaring subprograms.

**Test Benches:** Test benches, verifying responses, printing response values, reading data files.

**Verilog:** Overview of Digital Design with Verilog HDL, Basic Concepts, Modules and Ports, Basics of -Gate-Level Modeling, Dataflow Modeling, Behavioral Modeling.

**FPGA:** Introduction, Logic Block Architecture, Routing Architecture, Programmable, Interconnection, Design Flow, Xilinx Virtex-II , Artix-7 (Architecture), Boundary Scan, Programming FPGA's.

Interface of FPGA board with input and output devices.

**Laboratory Work:** Modelling and simulation of all VHDL and Verilog constructs using Model Sim, their testing by modelling and simulating test benches, Logic Synthesis using FPGA Advantage, Mapping on FPGA Boards.

### **Course learning outcomes (CLO):**

On completion of this course, the students will be able to:

1. develop a HDL code for a given logic circuit in various modeling styles.
2. design the digital systems using HDL subprograms.
3. verify the functionality of design by developing a test bench.
4. program the FPGA for a given combinational and sequential digital systems.

**Text Books:**

1. Charles H. Roth, Digital System Design Using VHDL , Jr., Thomson, (2008)2<sup>nd</sup> Ed.
2. Bhaskar, J., A VHDL Primer, Pearson Education/ Prentice Hall (2006)3<sup>rd</sup> Ed.

**Reference Books:**

1. Ashenden, P., The Designer's Guide To VHDL, Elsevier (2008) 3<sup>rd</sup> Ed.
2. David C. Black and Jack Donovan, SystemC: From the Ground Up, Springer, (2014) 2<sup>nd</sup> Ed.
3. Rushton, A., VHDL for Logic Synthesis, Wiley (1998) 2<sup>ed</sup>.
4. Samir Palnitkar, Verilog HDL: A Guide to Digital Design and Synthesis, Prentice Hall PTR (2003) 2<sup>nd</sup> Ed.

**Evaluation Scheme:**

S.No.	Evaluation Elements	Weightage (%)
1.	MST	25
2.	EST	45
3.	Sessionals (May include Assignments/Projects/Tutorials/Quizes/Lab Evaluations)	30

## PVL103: Digital VLSI Design

<b>L</b>	<b>T</b>	<b>P</b>
<b>3</b>	<b>1</b>	<b>2</b>

**Course Objectives:** To introduce the physics of MOSFETs, design rules of CMOS layout, basic theory of static and dynamic characteristics of CMOS logic circuits, power dissipation in CMOS logic circuits.

**Introduction:** Basic MOSFET Characteristics – Threshold Voltage, Body Bias concept, Current-Voltage Characteristics – Square-Law Model, MOSFET Modeling – Drain-Source Resistance, MOSFET Capacitances, Geometric Scaling Theory – Full-Voltage Scaling, Constant-Voltage Scaling, Challenges of MOSFET Scaling.

**Layout of CMOS Logic Circuits:** CMOS fabrication processing steps, Design Rules, Stick diagram, Layout of logic circuits, latch-up.

**Switching Properties of MOSFETs:** Static and dynamic characteristics of Pass Transistors, Transmission Gate, TG based logic circuits.

**CMOS Inverter:** Basic Circuit and DC Operation – DC Characteristics, Noise Margins, Layout considerations, Inverter Switching Characteristics, Transient Effects on the VTC, RC Delay Modeling, Elmore Delay, Output Capacitance, Inverter Design – DC Design, Transient Design, Driving Large Capacitive Loads.

**Static CMOS Logic Elements:** CMOS NAND Gate, CMOS NOR Gate, Complex Logic Functions, CMOS SRAM Cell.

**Power Dissipation in CMOS Digital Circuits:** Dynamic Power Dissipation – Switching Power Dissipation, Short Circuit Power Dissipation, Glitching Power Dissipation, Static Power Dissipation – Diode Leakage Current, Subthreshold Leakage Current.

**Dynamic Logic Circuit Concepts and CMOS Dynamic Logic Families:** Charge Leakage, charge Sharing, Dynamic RAM Cell, Clocked-CMOS, Pre-Charge/ Evaluate Logic, Domino Logic, Single-Phase Logic.

**Issues in Chip Design:** ESD Protection, On-Chip Interconnects – Line Parasitics, Modeling of the Interconnect Line, Clock Distribution, Input-Output circuits.

**Laboratory work:** Familiarization with schematic and layout entry using Mentor/ Cadence/ Tanner Tools, circuit simulation using SPICE; DC transfer Characteristics of Inverters, Transient response, Calculating propagation delays, rise and fall times, Circuit design of inverters, complex gates with given constraints; Circuit Simulation and Performance Estimation using SPICE; Layouts of CMOS circuits, Layout Optimization, Design Rule Check (DRC), Electrical Rule Check (ERC), Comparison of Layout Vs. Schematics, Circuit Extraction.



**Course Learning Outcomes:**

On completion of this course, the students will be able to:

1. synthesize and analyze the MOSFET based circuits.
2. draw the layout/stick diagram of CMOS logic circuits.
3. analyze the performance of CMOS logic circuits.
4. design CMOS combinational and dynamic logic circuits.

**Text Books:**

1. *Kang, S. and Leblebici, Y., CMOS Digital Integrated Circuits – Analysis and Design, Tata McGraw Hill (2008) 3rd ed.*
2. *J P Uyemura, CMOS Circuit Design, Springer*

**Recommended Books:**

1. *Weste, N.H.E. and Eshraghian, K., CMOS VLSI Design: A Circuits and Systems Perspective, Addison Wesley (1998) 2nd ed.*
2. *Baker, R.J., Lee, H. W. and Boyce, D. E., CMOS Circuit Design, Layout and Simulation, Wiley - IEEE Press (2004) 2nd ed.*
3. *Weste, N.H.E., Harris, D. and Banerjee, A., CMOS VLSI Design, Dorling Kindersley (2006) 3rd ed.*
4. *Rabaey, J.M., Chandrakasen, A.P. and Nikolic, B., Digital Integrated Circuits – A Design perspective, Pearson Education (2007) 2nd ed.*

**Evaluation Scheme:**

S.No.	Evaluation Elements	Weightage (%)
1.	MST	25
2.	EST	45
3.	Sessionals (May include Assignments/Projects/Tutorials/Quizes/Lab Evaluations)	30

## PVL206: Analog IC Design

L T P  
3 1 2

**Course Objectives:** To introduce analog MOS processes layout techniques, single stage amplifiers, working of operational amplifiers with frequency response, and noise impact.

**Basic MOSFET Physics:** IV Characteristics, Second order effects, MOS Device Models and Small Signal MOS Transistor Models.

**Analog MOS Process:** Analog CMOS Process (Double Poly Process), Digital CMOS Process tailored to Analog IC fabrication, Fabrication of active devices, passive devices and interconnects, Analog Layout Techniques, Symmetry, Multi-finger transistors, Passive devices: Capacitors and Resistors, Substrate Coupling, Ground Bounce.

**Amplifiers and Current sources:** Large Signal and Small-Signal analysis of common source stage, Source Follower, Common Gate Stage, Cascode, Folded Cascode, differential amplifier, current Sources, Basic Current Mirrors, Cascode Current Mirrors and current mirror based differential amplifier.

**Frequency Response of Amplifiers:** Miller Effect, Association of Poles with nodes, Frequency Response of all single stage amplifiers.

**Voltage References:** Different Configurations of Voltage References, Major Issues, Supply Independent Biasing, Temperature-Independent References.

**Feedback:** General Considerations, Topologies, Effect of Loading.

**Operational Amplifier:** General Considerations, Theory and Design, Performance Parameters, Design of 2-stage MOS Operational Amplifier, Gain Boosting, slew rate, Offset effects, PSRR, Stability and Frequency Compensation, topologies, familiarity with non linearity and mismatch

**Noise:** Noise Spectrum, Sources, Types, Thermal and Flicker noise, Representation in circuits, Noise Bandwidth, Noise Figure.

**Laboratory work:** Review of Mentor Tools; Analysis of Various Analog Building Blocks such as, Current and Voltage References/Sources, Current Mirrors, Differential Amplifier, Design and Analysis of Op-Amp, Analog Layout Constraints, Layout Designs and Analysis.

### Course Learning Outcomes:

On completion of this course, the students will be able to:

1. acquire a basic knowledge of analog IC design including small signal models, analog MOS processes and layout techniques.
2. design of single stage and differential stage amplifiers with and without current mirror circuits, respectively.
3. analyze the frequency responses of single stage amplifiers .
4. analyze and design two-stage operational amplifier
5. identify the different types of noises in analog integrated circuits.

**Recommended Books:**

1. *Razavi, B., Design of Analog CMOS Integrated Circuits, Tata McGraw Hill (2008).*
2. *Gray, P.R., Hurst, P.J., Lewis, S.H., and Meyer, R.G., Analysis and Design of Analog Integrated Circuits, John Wiley (2001) 5th ed.*
3. *Allen, P.E. and Holberg, D.R., CMOS Analog Circuit Design, Oxford University Press (2002) 2nd ed.*
4. *Gregorian, R. and Temes, G.C., Analog MOS Integrated Circuits for Signal Processing, John Wiley (2004).*
5. *Hastings, A., The Art of Analog Layout, Prentice Hall (2005).*

**Evaluation Scheme:**

S.No.	Evaluation Elements	Weightage (%)
1.	MST	25
2.	EST	45
3.	Sessionals (May include Assignments/Projects/Tutorials/Quizes/Lab Evaluations)	30

## PVL203 VLSI SIGNAL PROCESSING

<b>L</b>	<b>T</b>	<b>P</b>
<b>3</b>	<b>0</b>	<b>0</b>

**Course objective:** To know how to design high-speed, low-area, and low-power VLSI systems for a broad range of DSP applications. Explore optimization techniques indispensable in modern VLSI signal processing. Immediate access to state-of-the-art, proven techniques for designers of DSP applications- in wired, wireless, or multimedia communications.

**Introduction:** Review of IIR and FIR Filters, Multirate Signal Processing: Sampling rate conversion by rational factors, Implementation of sampling rate conversion, Multistage Implementation, Applications of multirate signal processing, Digital filter banks, Wavelets, Introduction to DSP Systems, Graph Theoretic Representation of DSP programs, Data Flow graphs (DFGs), Single rate and multi rate DFGs, Iteration bound, Loop, Loop Bound, Iteration rate, Critical loop, Critical path analysis, Area-Speed-Power trade-offs, Precedence constraints, Acyclic Precedence graph, Longest Path Matrix (LPM) and Minimum Cycle Mean (MCM) Algorithms, Pipelining and parallel processing of DSP Systems, Pipelining and parallel processing for Low Power Consumption.

**Algorithmic Transformations:** Retiming, Cut-set retiming, Feed-Forward and Feed-Backward, Clock period minimization, register minimization, Unfolding, Sample period reduction, Parallel processing, Bit-serial, Digit-serial and Parallel Architectures of DSP Systems, Folding, Folding order, Folding Factor, Folding Bi-quad filters, Retiming for folding, Register Minimization technique, Forward Backward Register Allocation technique.

**Systolic Architecture Design and Fast Convolution:** Systolic architecture design methodology, Projection vector, Processor Space vector, Scheduling vector, Hardware Utilization efficiency, Edge mapping, Design examples of systolic architectures, Cook-Toom Algorithm, Winograd Algorithm, Iterated Convolution, Cyclic Convolution.

**Algorithm Strength Reduction:** Introduction, Parallel FIR filters, Polyphase decomposition, Fast FIR filters Algorithms, Discrete Cosine Transform and Inverse Discrete Cosine Transform, Algorithm-Architecture Transformation, DIT Fast DCT, Pipelined and Parallel Recursive, Look-Ahead Computation, Look-Ahead Pipelining, Decompositions, Clustered Look-Ahead Pipelining, Scattered Look-Ahead pipelining, Parallel processing in IIR Filters

**Distributed Arithmetic and Signal processing for Machine Learning :** Distributed Arithmetic (DA) for MAC circuits, Efficient Resource utilization using Distributed Arithmetic, Area efficient hardware realization using DA, Convolution Neural Networks (CNNs), Winograd filtering based CNN for VLSI implementation.

### **Course learning outcome (CLO):**

On completion of this course, the students will be able to:

1. analyze signal processing tasks from VLSI perspective
2. perform the algorithmic transformations using pipelining, retiming, parallel processing techniques for the development of high speed and lower systems,
3. develop area efficient systems using folding and distributed arithmetic approaches.
4. utilize efficient signal processing techniques for VLSI implementation of machine learning tasks.

***Text Books:***

1. *Parhi, K.K., VLSI Digital Signal Processing Systems: Design and Implementation, John Wiley (2007).*
2. *Oppenheim, A.V. and Schafer, R.W., Discrete-Time Signal Processing, Prentice Hall (2009) 2<sup>nd</sup> ed.*

***Reference Books:***

1. *Proakis, J.G., Digital Filters: Analysis, Design and Application, McGraw Hill (1981) 2nd ed.*
2. *Proakis, J.G., and Manolakis, D.G., Digital Signal Processing, PHI (2001) 3rd ed.*
3. *Mitra, S.K., Digital Signal Processing. A Computer Based Approach, McGraw Hill (2007) 3<sup>rd</sup> ed.*

**Evaluation Scheme:**

S.No.	Evaluation Elements	Weightage (%)
	MST	30
	EST	45
	Sessionals (Assignments+Quizes)	25

## PVL: EMBEDDED SYSTEMS DESIGN

L T P  
3 0 2

**Course Objective:** To understand the basic concepts of embedded system, understanding of different types of programming languages used for embedded systems. Study of ARM based processors: architecture, programming and interfacing of ARM processor with memory & I/O devices. To discuss the features, Architecture and programming of Arduino Microcontroller, Architecture of Arduino. To study of RTOS.

### **Course Content Details:**

**Introduction to Embedded Systems:** Background and History of embedded systems, Definition and Classification, Von-Neuman and Harvard architectures, Processor design trade-offs, CISC and RISC architectures, Programming languages for embedded systems, Embedded Systems on a Chip (SoC) and the use of VLSI designed circuits.

**ARM Processor Fundamentals and pipeline structure:** ARM Architecture, ARM General purpose Register set and GPIO's, CPSR, Pipeline, Exceptions, Interrupts, Vector Table, ARM processors family, ARM core data flow model, ARM 3 stage Pipeline, ARM family attribute comparison. ARM 5 stage Pipeline, Pipeline Hazards, Data forwarding

**ARM7TDMI Processor assembly instructions:** ARM instruction set. ARM programming in Assembly, in C and C++ Instruction Scheduling, Conditional Execution, Looping Constructs, Bit Manipulation, Exception and Interrupt Handling. Thumb state, Thumb instruction set, Thumb Programmers model, Thumb Applications, ARM coprocessor interface and Instructions, Coprocessor Instructions.

**ARM tools and Peripherals:** ARM Development Environment, Arm Procedure Call Standard (APCS), Example C/C++ programs, Embedded software Development, Image structure, linker inputs and outputs, Protocols (I<sup>2</sup>C, SPI), GPIO, ARM systems with MPU, memory Protection Unit (MPU). Physical Vs Virtual Memory, Paging, Segmentation. AMBA Overview, Typical AMBA Based Microcontroller, AHB bus features, AHB Bus transfers, APB bus transfers, APB bridge. Introduction to Arduino and Raspberry pi.

**Real Time Operating Systems (RTOS):** Architecture of an RTOS, Important features of Linux, Locks and Semaphores, Operating System Timers and Interrupts, Exceptions, Tasks: Introduction, Defining a task, Task states and scheduling, Task structures, Synchronization, Communication and concurrency, Kernel objects: Semaphores, Queues.

**Laboratory Work:** Introduction to ARM processor kit, Programming examples of ARM processor. Interfacing of LED, seven segment display, ADC and DAC with ARM processor. Raspberry Pi based projects.

**Course Learning Outcomes (CLOs):**

On completion of this course, the students will be able to:

- recognize the need of Embedded system and System on a Chip (SoC).
- identify the internal Architecture and perform the programming of ARM processor.
- apply the concept of Thumb mode operation and interfacing of coprocessors in an embedded system.
- interface AMBA bus architecture, various HW peripherals in embedded systems and how memory mapping can be done.
- analyze the need of Real time Operating System (RTOS) in embedded systems.

**Text Books**

1. Steve Furber, “ARM System-on-Chip Architecture, Second Edition, PEARSON, 2013.
2. Andrew N. Sloss, *ARM System Developer’s Guide Designing and Optimizing System Software*, Morgan Kaufman Publication (2010).

**Reference Books**

1. Simon, D.E., *An Embedded Software Primer*, Dorling Kindersley (2005).
2. Alan G. Smith, *Introduction to Arduino: A piece of cake*, CreateSpace Independent Publishing Platform (2011).
3. *User manual of Raspberry pi and Red Pitaya embedded board.*
4. Michael McRoberts, *Beginning Arduino, Technology in action publications*, 2<sup>nd</sup> Edition.

**Evaluation Scheme:**

S. No.	Evaluation Elements	Weightage (%)
4.	MST	25
5.	EST	45
6.	Sessionals (May include Assignments/Projects/Tutorials/Quizes/Lab Evaluations)	30

## PVL212: Physical Design Automation

L T P  
3 1 0

**Course Objectives:** In this course the students will learn VLSI Cad tools and its related concepts, algorithms, Design automation of FPGA and high level synthesis.

**Introduction to VLSI Design:** Automation, use of VLSI CAD tools, Algorithmic Graph Theory, Computational Complexity and ROBDD; Partitioning and Placement: KL algorithm, FM algorithm, Group-migration algorithm, Simulated Annealing and Evolution

**Floor planning and Pin Assignment** Placement, Layout styles, Discrete methods in global placement, Timing-driven placement, Routing: Global Routing, detailed routing, Graph models, Line Search, Maze Routing, Channel Routing, Steiner Tree based Algorithms, ILP base approaches

**Performance Issues in circuit layout:** delay models, timing driven placements, timing driven routing, Via Minimization, Over the Cell Routing – Single layer and Two layer routing, Clock and Power Routing

**Compaction :** Problem formulation, One Dimension compaction, Two Dimension compaction, Hierarchical Compaction, Compaction Algorithms. Physical Design Automation in FPGAs

**High level synthesis:** Introduction to HDL, HDL to DFG, operation scheduling: constrained and unconstrained scheduling, ASAP, ALAP, List scheduling, Force directed Scheduling, operator binding, Static Timing ANalyss: Delay models, setup time, hold time, cyvcle time, critirical paths, Topological mvs. Logical timing analuysis, False paths, Arrival time (AT), Required arrival Time (RAT), Slacks.

### Course Learning Outcomes:

The student will be able to

1. Understand of VLSI Design Automation.
2. Acquire knowledge about CAD tools used for VLSI design.
3. Able to understanding Algorithms for VLSI Design Automation.
4. Able to gather knowledge of High Level Synthesis.
5. Understand Timing Analysis

### Recommended Books:

1. *Sherwani, N., Algorithms for VLSI Physical Design Automation, Springer (2005) 3<sup>rd</sup> ed.*
2. *Gerez S.H., Algorithms for VLSI Design Automation, John Wiley (1998)*
3. *Sarrafzadeh, M. and Wong, C. K., An Introduction to VLSI Physical Design, McGraw Hill (1996).*
4. *Trimberger, S. M., An Introduction to CAD for VLSI, Kluwer (1987).*
5. *Sait, S. M. and Youssef, Habib, VLSI Physical Design Automation – Theory and Practice, World Scientific, 2004.*

### Evaluation Scheme:



S.No.	Evaluation Elements	Weightage (%)
1.	MST	30
2.	EST	45
3.	Sessionals (May include Assignments/Projects/Tutorials/Quizes/Lab Evaluations)	25

## PVL208: VLSI Testing and Verification

L T P  
3 0 2

**Course Objective:** In this course students will learn test economics, fault modelling, logic and fault simulation, ATPG concepts for combinational and sequential circuits. Students will also be able to write testbenches for the complex VLSI design using System Verilog.

**Introduction:** Role of testing in VLSI design, Issues in test and verification of complex chips, VLSI test process and equipment, Test economics, Yield analysis and product quality.

**Faults modelling and fault simulation:** Physical faults and their modelling, Stuck-at faults, Bridging faults, Fault collapsing, Fault simulation, Deductive, Parallel and Concurrent fault simulation, Combinational and sequential SCOAP measures.

**ATPG for combinational circuits:** D-Algorithm, Boolean Difference, PODEM, Random, Exhaustive and Weighted Test Pattern Generation, Alias

g and its effect on Fault coverage.

**ATPG for sequential circuits:** ATPG for Single-Clock Synchronous Circuits, Time frame expansion method, Simulation-Based Sequential Circuit ATPG.

**Memory testing and BIST:** Permanent, Intermittent and pattern sensitive faults, March test notion, Memory testing using march tests, PLA testing, Ad-Hoc DFT methods, Scan design, Partial scan design, Random logic for BIST, Memory BIST.

**Verification:** Design verification techniques based on simulation, Analytical and formal approaches, Functional verification, Timing verification, Formal verification, Basics of equivalence checking and model checking, Hardware emulation.

**Hardware verification language:** Introduction to System Verilog, Development of stimulus generator, Monitor and complete test bench using System Verilog.

### **Laboratory Work:**

Familiarization with development of testbenches using Verilog/SystemVerilog on Mentor/Cadence/Xilinx-ISE tools, Logic simulation, Logic level diagnosis, ATPG, development of verification plan for the given design and writing testcases, computation of fault-coverage/code-coverage index.

### **Text Books:**

1. M. Bushnell and Vishwani Agrawal, Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits, Springer, ISBN 978-0792379911.
2. Chris Spear, System Verilog for Verification, Springer, ISBN 978-1-4614-0714-0

### **Reference Books:**

1. M. Abramovici, M. Breuer, and A. Friedman, *Digital System Testing and Testable Design*, IEEE Press, 1994
2. Diraj K. Pradhan, "Fault Tolerant Computer System Design", Prentice Hall.
3. L. T. Wang, C. W. Wu, and X. Wen, *VLSI Test Principles and Architectures*, Morgan Kaufmann, 2006, ISBN-13: 978-0-12-370597-6, ISBN-10: 0-12-370597-5.
4. *System-on-a-Chip Verification-Methodology and Techniques*, P. Rashinkar, Paterson and L. Singh, Kluwer Academic Publishers, 2001
5. Janick Bergeron, "Writing test benches functional verification of HDL models" Kluwer Academic Publishers, New York, Boston, Dordrecht, London, Moscow, 2002.

**Course Learning Outcomes:**

The student will be able to

1. Acquire knowledge about fault modelling and collapsing.
2. Learn about various combinational automatic test pattern generation techniques.
3. Learn about various sequential automatic test pattern generation techniques.
4. Analyze different memory faults and its testing methods.
5. Develop the verification plan for the small to complex VLSI designs.
6. Develop testbench using HVL for testing and verification of VLSI designs.

**Evaluation Scheme:**

S.No.	Evaluation Elements	Weightage (%)
1.	MST	25
2.	EST	45
3.	Sessionals (May include Assignments/Projects/Tutorials/Quizes/Lab Evaluations)	30

## PVL\*\*\*: CAD for VLSI Design

**L T P**  
**3 0 2**

**Course Objectives:** In this course the students will learn about the VLSI design flow, supporting CAD environment and importance of CAD in VLSI design flow.

**Introduction to Unix:** Architecture, Basic commands, General Purpose utilities, File System, Handling Files, File Attributes, vi editor, regular expression, shell scripting, awk and grep.

**Perl:** Introduction to Perl, Literals, Variable types and contexts, Perl Arrays, Perl Hashes, Operators, Conditionals, Loops & Subroutines, Files and File handling, Directory, Pattern Matching and Regular Expressions, Accessing System Resources, Generating Reports with Perl.

**Python:** Introduction to Python, Fundamentals to Python, operators and conditions, regular expressions, Loops, working with files, Arguments, modules.

**Laboratory Work:** Writing basic commands in unix, perl and python. Also write programs in unix, perl and python.

**Course learning outcome (CLO):** The student will be able to

1. acquire the basic knowledge of unix commands and programming skills.
2. learn the basics of perl and python.
3. acquire the basic knowledge to write programs in perl and python.

### Text Books:

1. Sumitbha Das, Unix: Concepts And Applications, McGraw Hill Education, 4<sup>th</sup> edition.
2. Ellie Quigley, Perl by Example, Prentice Hall, 5<sup>th</sup> edition, 2014.
3. Mark Lutz, Learning Python, O'Reilly Media, 5<sup>th</sup> edition, 2013.

### Evaluation Scheme:

S.No.	Evaluation Elements	Weightage (%)
1.	MST	25
2.	EST	45
3.	Sessionals (May include Assignments/Projects/Tutorials/Quizes/Lab Evaluations)	30

## PVL224: MOS Device Modeling

L T P  
3 0 2

**Course Objectives:** In this course the students will learn fundamental of semiconductor physics, quantum mechanics, carrier transport, MOSFET modelling and its analysis.

**Semiconductor Fundamentals:** Poisson and Continuity Equations, Recombination, Equilibrium carrier concentrations (electron statistics, density of states, effective mass, band gap narrowing, Review of PN and MS diodes).

**Quantum Mechanics Fundamentals:** Basic Quantum Mechanics, Crystal symmetry and band structure, 2D/1D density of states, Tunneling.

**Modeling and Simulation of Carrier Transport:** Carrier Scattering (impurity, phonon, carrier-carrier, remote/interface), Boltzmann Transport Equation, Drift-diffusion.

**MOS Capacitors:** Modes of operation (accumulation, depletion, strong/weak inversion), Capacitance versus voltage, Gated diode, Non-ideal effects (poly depletion, surface charges), High field effects (tunneling, breakdown).

**MOSFET Modeling:** Introduction Interior Layer, MOS Transistor Current, Threshold Voltage, Temperature Short Channel and Narrow Width Effect, Models for Enhancement, Depletion Type MOSFET, CMOS Models in SPICE, Long Channel MOSFET Devices, Short Channel MOSFET Devices.

**Parameter Measurement:** General Methods, Specific Bipolar Measurement, Depletion Capacitance, Series Resistances, Early Effect, Gummel Plots, MOSFET: Long and Short Channel Parameters, Statistical Modeling of Bipolar and MOS Transistors.

**Advanced Device Technology:** SOI, SiGe, strained Si, Alternative oxide/gate materials, Alternative geometries (raised source/drain, dual gate, vertical, FinFET), Memory Devices (DRAM, Flash). Sub-micron and Deep sub-micron Device Modeling.

### Course Learning Outcomes:

The student will be able to

1. Acquire knowledge about physics involved in modelling of semiconductor device.
2. Acquire the basic knowledge about quantum mechanical fundamentals.
3. Model MOSFET devices.
4. Identify characteristics of Advanced Device Technology

### Recommended Books:

1. *Tsividis, Y., Operation and Modeling of the MOS Transistor, Oxford University Press, (2008) 2nd ed.*
2. *Sze, S.M., Physics of Semiconductor Devices, Wiley (2008).*
3. *Muller, R.S., Kamins, T.I., and Chan, M., Device Electronics for Integrated Circuits, John Wiley (2007) 3rd ed.*

4. *Taur, Y. and Ning, T.H., Fundamentals of Modern VLSI Devices, Cambridge University Press (2009).*
5. *Massobrio, G. and Antognetti, P., Semiconductor Device Modeling, McGraw Hill (1998).*

**Evaluation Scheme:**

S.No.	Evaluation Elements	Weightage (%)
1.	MST	25
2.	EST	45
3.	Sessionals (May include Assignments/Projects/Tutorials/Quizes/Lab Evaluations)	30

## PVL207: Low Power System Design

L T P  
3 0 2

**Course objective:** To understand the causes of the power dissipation in digital ICs, quantitative analysis of power dissipation in VLSI circuits and exploring the low power circuits and architectures for VLSI system.

**Introduction:** Need for low power VLSI chips, Sources of power dissipation on Digital Integrated circuits. Emerging Low power approaches. Physics of power dissipation in CMOS devices.

**Sources of Power Dissipation:** Dynamic dissipation in CMOS, Transistor sizing & gate oxide thickness, Impact of technology Scaling, Technology & Device innovation.

**Power estimation, Simulation Power analysis:** SPICE circuit simulators, gate level logic simulation, capacitive power estimation, static state power, gate level capacitance estimation, architecture level analysis, Monte Carlo simulation.

**Probabilistic power analysis:** Random logic signals, probability & frequency, probabilistic power analysis techniques, signal entropy.

**Low Power circuit level Design:** Power consumption in circuits. Flip Flops & Latches design, high capacitance nodes, low power digital cells library, logic level, Gate reorganization, signal gating, logic encoding, state machine encoding, pre-computation logic

**Leakage Power Minimization Approaches:** Variable threshold voltage CMOS (VTCMOS) approach. Multi-threshold-voltage CMOS (MTCMOS), Dual-Vt assignment approach (DTCMOS), Transistor stacking.

**Low Power Static RAM Architecture:** Architecture of SRAM array, Reduced Voltage Swings on Bit Lines, Reducing power in memory peripheral circuits

### Text/References:

1. Gary K. Yeap, "Practical Low Power Digital VLSI Design", KAP, 2002
2. Kaushik Roy, Sharat Prasad, "Low-Power CMOS VLSI Circuit Design" Wiley,
3. Rabaey, Pedram, "Low power design methodologies" Kluwer Academic, 1997
4. Anantha Chandrakasan and Robert Brodersen, "Low Power CMOS Design" Standard Pub., 1995

### Course Learning Outcomes:

The student will be able to:

1. Understand the need for low power in VLSI.
2. Understand various dissipation types in CMOS.

3. Estimate and analyse the power dissipation in VLSI circuits.
4. Understand the probabilistic power techniques.
5. Derive the architecture of low power SRAM circuit.

**Evaluation Scheme:**

S.No.	Evaluation Elements	Weightage (%)
1	MST	25
2.	EST	45
3.	Sessionals (May include Assignments/Projects/Tutorials/Quizes/Lab Evaluations)	30



## PVL230: System C

**L T P**  
**3 0 2**

**Course Objectives:** The objective of this course is to provide methods and techniques to develop the Electronic System Design using System C. Also, it will be used to model the behaviour of any electronic system.

**Introduction:** Overview, Design methodology, capabilities and System C-RTL.

**Data types:** Value Holders, Summary of types, bit type, Logic type, Signed integer, unsigned integer, resolved and user defined types.

**Modeling of Combinational Logic:** File structures, Reading and writing ports, signals, logic operators, arithmetic operators-unsigned, signed, relational operators, vectors and ranges, if statement, switch statement, loops, methods, structures, multi processes and delta delays.

**Modeling of Synchronous Logic:** Modeling flip-flops, multiple processes, flip-flop with asynchronous and synchronous Present and Clear, multiple and multi-phase clocks, modeling and avoiding latches.

**Miscellaneous Logic and Modeling examples:** Three-state drivers, multiple drivers, handling don't cares, hierarchy, parameterizing modules, variable assignments, signal assignments, Parameterizable Register with three-state output, a memory model, modeling of FSM, shift register-universal and counters.

**Test Benches:** Overview, simulation control, waveforms and monitoring behaviour.

**Laboratory Work:** Modeling and simulation of blocks and complete System design using System C.

**Course learning outcome (CLO):** The student will be able to:

1. acquire the knowledge of different data types.
2. model the combinational logic using system C.
3. model the synchronous logic using system C.
4. verify the functionality of design by developing a test bench code.

### Text Books:

1. J. Bhasker, *A SystemC Primer*, Star Galaxy Publishing, Second Edition, 2010
2. David Black, Jack Donovan, Bill Bunton and Anna Keist, *SystemC: From the Ground Up*, Springer, Second Edition, 2009.

**Evaluation Scheme:**

S.No.	Evaluation Elements	Weightage (%)
1.	MST	25
2.	EST	45
3.	Sessionals (May include Assignments/Projects/Tutorials/Quizes/Lab Evaluations)	30

## PEC339: IMAGE PROCESSING AND COMPUTER VISION

L T P  
3 0 2

**Course objective:** To make students to understand image fundamentals and how digital images can be processed, Image enhancement techniques and its application, Image compression and its applicability, fundamentals of computer vision, geometrical features of images, object recognition and application of real time image processing.

**Introduction:** Digital image representation, fundamental steps in image processing, elements of digital image processing systems digitization.

**Digital Image Fundamentals:** A Simple Image Model, Sampling and Quantization, Relationship between Pixel, Image Formats and Image Transforms.

**Image Enhancement:** Histogram processing, image subtraction, image averaging, smoothing filters, sharpening filters, enhancement in frequency and spatial domain, low pass filtering, high pass filtering.

**Image Compression:** Fundamentals, Image Compression Models, Elements of Information Theory, Error-Free Compression, Lossy Compression, Recent Image Compression Standards.

**Real Time Image Processing:** Introduction to Digital Signal Processor (TMS320CXX), Introduction to Texas Instruments Image Library, Development of a real time image processing algorithms.

**Computer Vision:** Imaging Geometry, Coordinate transformation and geometric warping for image registration, Hough transforms and other simple object recognition methods, Shape correspondence and shape matching, Principal Component Analysis, Shape priors for recognition, Implementation of computer vision algorithms using Raspberry Pi.

### Laboratory Work:

1. Introduction to Image Processing Toolbox of Python and MATLAB®.
2. Sampling and Quantizing Images.
3. Histogram of Images, Contrast Enhancement.
4. Filtering of Images.
5. Geometrical transformations on Images.

**Minor Project:** Image Compression and Facial Feature Detection with FPGA/ASIC/ARM/DSP Processors.

### Course learning outcomes (CLOs):

The students will be able to

- Recognize the fundamental techniques of Image Processing and Computer Vision.
- Interpret the basic skills of designing image compression.

- Distinguish between different image compression standards.
- Analyse different computer vision techniques
- Analyse real time image processing system.

**Text Books:**

1. *Gonzalez, R.C., and Woods, R.E., Digital Image Processing, Dorling Kingsley (2009) 3rd Ed.*
2. *Jain A.K., Fundamentals of Digital Image Processing, Prentice Hall (2007).*
3. *Sonka M., Image Processing and Machine Vision, Prentice Hall (2007) 3rd Ed.*
4. *D. Forsyth and J. Ponce, Computer Vision - A modern approach, Prentice Hall.*
5. *B. K. P. Horn, Robot Vision, McGraw-Hill.*
6. *E. Trucco and A. Verri, Introductory Techniques for 3D Computer Vision, Prentice Hall.*

**Reference Books:**

1. *Tekalp A.M., Digital Video Processing, Prentice Hall (1995).*
2. *Ghanbari M., Standard Codecs: Image Compression to Advanced Video Coding, IET Press (2003).*

**Evaluation Scheme:**

S.No.	Evaluation Elements	Weightage (%)
1.	MST	25
2.	EST	45
3.	Sessionals (May include Assignments/Projects/Tutorials/Quizes/Lab Evaluations)	30

## PVL332: Mixed Signal Circuit Design

L T P  
3 0 0

**Course Objectives:** In this course the students will learn basics of comparator circuits, data converters, implementation of A/D and D/A converters and their performance analysis with design challenges.

**Introduction:** Device Models, IC Process for Mixed Signal, Concepts of MOS Theory.

**Comparators:** Circuit Modeling, Auto Zeroing Comparators, Differential Comparators, Regenerative Comparators, Fully Differential Comparators, Latched Comparator.

**Data Converters:** Requirements, Static and Dynamic Performance, SNR and BER, DNL, INL.

**High Speed A/D Converter Architectures:** Flash, Folding, Interpolating, pipelined

**High Speed D/A Converter Architectures:** Nyquist-Rate D/A Converters, Thermometer Coded D/A Converters, Binary Weighted D/A Converters.

**Design** of multi channel low level and high level data acquisition systems using ADC/DAC, SHA and Analog multiplexers, Designing of low power circuits for transducers.

**Sigma-Delta Data Converter Architectures:** Programmable Capacitor Arrays (PCA), Switched Capacitor converters, Noise Spectrum, Sigma-Delta Modulation Method, Sigma-Delta A/D and D/A Converters, Non Idealities.

**Key Analog Circuit Design:** Analog VLSI building blocks, Operational Amplifiers for converters, advanced op-amp design techniques, Voltage Comparators, Sample-and-Hold Circuits.

**Implementation and Design of High Performance A/D and D/A Converters:** System Design, Digital Compensation, Noise, and Mismatch, Layout and Simulation Technologies for Data Converters.

**Design Challenges:** Low Voltage Design, Ultra-High Speed Design, High Accuracy Design.

**Advanced Topics:** Multipliers, Oscillators, Mixers, Passive Filter Design, Active filter design, Switched Capacitor Filters, Frequency Scaling, Phase-Locked Loops, Device Modeling for AMS IC Design, Concept of AMS Modeling and Simulation.

### Course Learning Outcomes:

The student will be able to

1. Apply knowledge of mathematics, science, and engineering to design CMOS analog circuits to achieve performance specifications.
2. Identify, formulate, and solve engineering problems in the area of mixed-signal design.
3. Use the techniques and skills for design and analysis of CMOS based switched capacitor circuits.
4. Work as a team to design, implement, and document a mixed-signal integrated circuit.

**Recommended Books:**

1. *Baker, R.J., Li, H.W. and Boyce, D.E., CMOS: Circuit Design, Layout and Simulation, IEEE Press (2007) 2nd ed.*
2. *Gregorian, R. and Temes, G.C., Analog MOS Integrated Circuits for Signal Processing, Wiley (2002).*
3. *Gregorian, R., Introduction to CMOS Op-Amps and Comparators, Wiley (1999).*
4. *Jespers, P.G. A., Integrated Converters: D-A and A-D Architectures, Analysis and Simulation, Oxford University Press (2001).*
5. *Plassche, Rudy J. Van De, Integrated A-D and D-A Converters, Springer (2007), 2nd ed.*

**Evaluation Scheme:**

S.No.	Evaluation Elements	Weightage (%)
1.	MST	30
2.	EST	45
3.	Sessionals (May include Assignments/Projects/Tutorials/Quizes/Lab Evaluations)	25

## PVL331: Memory Design and Testing

L T P  
3 0 0

**Course Objectives:** In this course the students will learn overview of memory chip design, DRAM circuits, voltage generators, performance analysis and design issues of ultra-low voltage memory circuits.

**Introduction to Memory Chip Design:** Basics of Semiconductor Memory, Internal Organization of Memory Chips, Memory Cell Array, Peripheral Circuit, I/O Interface Categories of Memory Chip, History of Memory-Cell Development, Architectures of memory cell: SRAM Cell, DRAM Cell Trends in Non-Volatile Memory Design and Technology, Ferroelectric memory, Basic Operation of Flash Memory Cells, Advances in Flash-Memory Design and Technology.

**Basics of RAM Design and Technology:** Devices, NMOS Static Circuits, NMOS Dynamic Circuits, CMOS Circuits, Basic Memory Circuits, Scaling Law.

**DRAM Circuits:** High-Density Technology, High-Performance Circuits, Catalog Specifications of the Standard DRAM, Basic Configuration and Operation of the DRAM Chip, Chip Configuration, Address Multiplexing, Fundamental Chip, Multi-divided Data Line and Word Line, Read and Relevant Circuits, Write and Relevant Circuits, Refresh-Relevant Circuits, Redundancy Techniques, On-Chip Testing Circuits, High Signal-to-Noise Ratio DRAM Design and Technology, Trends in High S/N Ratio Design, Data-Line Noise Reduction, Noise Sources.

**On-Chip Voltage Generators:** Substrate-Bias Voltage (VBB) Generator, Voltage Up Converter, Voltage Down-Converter, Half-VDD Generator, Examples of Advanced On-Chip Voltage Generators.

**High-Performance Subsystem Memories:** Hierarchical Memory Systems, Memory-Subsystem Technologies, High-Performance Standard DRAMs, Embedded Memories. Low-Power Memory Circuits: Sources and Reduction of Power Dissipation in a RAM Subsystem and Chip, Low-Power DRAM Circuits, Low-Power SRAM Circuits.

**Ultra-Low-Voltage Memory Circuits:** Design Issues for Ultra-Low-Voltage RAM Circuits, Reduction of the Subthreshold Current, Stable Memory-Cell Operation, Suppression of, or Compensation for, Design Parameter Variations, Power-Supply Standardization, Ultra-Low Voltage DRAM Circuits, Ultra-Low-Voltage SRAM Circuits, Ultra-Low-Voltage SOI Circuits.

**Radiation Effects in semiconductor memories.**

### Course Learning Outcomes:

The student will be able to

1. Acquire knowledge about Basics of memory chip Design and Technology.
2. Acquire knowledge about RAM and DRAM Design.
3. Know about On-Chip Voltage Generators.
4. Work using Laplace Trans., CTFT and DTFT.
5. Acquire knowledge about High-Performance Subsystem Memories

### Recommended Books:

1. Itoh, K., *VLSI Memory Chip Design*, Springer (2006).

2. *Sharma, A. K., Semiconductor Memories: Technology, Testing and Reliability, Wiley- IEEE press (2002).*
3. *Adams, R. D., High performance Memory Testing: Design Principles, Fault Modeling and Self-Test, Springer (2002).*
4. *Sharma, A. K., Advanced Semiconductor Memories: Architecture, Design and Applications, John Wiley (2002).*
5. *Prince, B., Semiconductor Memories: A handbook of Design, Manufacture and Application, John Wiley (1996) 2nd ed.*

**Evaluation Scheme:**

S.No.	Evaluation Elements	Weightage (%)
1.	MST	30
2.	EST	45
3.	Sessionals (May include Assignments/Projects/Tutorials/Quizes/Lab Evaluations)	25



## PVL110 : VLSI Architectures

L T P  
3 0 0

**Course objective:** The motive of this course is to inculcate the knowledge of the different processors; their architecture and organizational intricacies. For performance enhancement consideration is given to various instruction level and memory management techniques such as pipelining ,parallelism, instruction scheduling, hierarchical memory management etc. Study of the superscaler architecture organization, design issues and Power PCs is to be carried out.

**Introduction:** Review of basic computer architecture, quantitative techniques in computer design, measuring and reporting performance. CISC and RISC processors. Processor organization and Architectural Overview.

**Pipelining:** Basic concepts, instruction and arithmetic pipeline, data hazards, control hazards, and structural hazards, techniques for handling hazards. Exception handling. Pipeline optimization techniques, dynamic instruction scheduling

**Hierarchical memory technology:** Inclusion, Coherence and locality properties; Cache memory organizations, Techniques for reducing cache misses; Virtual memory organization, mapping and management techniques, memory replacement policies.

**Instruction-level parallelism:** basic concepts, techniques for increasing ILP, superscalar, super-pipelined and VLIW processor architectures. Array and vector processors.

**Multiprocessor architecture:** taxonomy of parallel architectures. Centralized shared-memory architecture: synchronization, memory consistency, interconnection networks. Distributed shared-memory architecture Superscaler Processors: Overview, Design Issues, PowerPC, Pentium

### Course Learning Outcome (CLO):

The students will able to:

- 1.To review the basics of different processors including architecture and organization
- 2.To foster ability of handling and designing different types of pipelining techniques; exception handling corresponding instruction scheduling.
- 3.To understand various memory organization and management techniques
- 4.To Understand the various advanced architectures.
- 5.To achieve the understanding of parallel, shared architectures and important organizational details of superscaler architecture

### Text Books:

1. *Hennessy, J.L., Patterson, D.A, and Goldberg, D., Computer Architecture A Quantitative Approach, Pearson Education Asia (2006) 4th ed.*
2. *Leigh, .E. and Ali, D.L., System Architecture: software and hardware concepts, South Wester Publishing Co. (2000).*

3. *Stallings, W., Computer Organization and Architecture: Designing for Performance, Prentice Hall (2003) 7th ed.*
4. *Parhami, B., Computer Arithmetic Algorithms and Hardware Design, Oxford (2000).*

**Reference Books:**

1. *Mano, Morris M., Computer System Architecture, Prentice Hall (2013), 5th ed.*
2. *Hayes, J.P., Computer Architecture and Organization, McGraw Hill (1998) 3rd ed.*

**Evaluation Scheme:**

S.No.	Evaluation Elements	Weightage (%)
•	MST	30
•	EST	45
•	Sessionals (May include Assignments/Projects/Tutorials/Quizes/Lab Evaluations)	25

## PVL344: Hardware Algorithms for Computer Arithmetic

L T P  
3 0 0

**Course Objectives:** In this course the students will learn redundant number systems, algorithms for fast addition, VLSI implementation aspects, High speed multiplication, VLSI layout considerations, algorithms for fast division and impact of hardware technology.

**Numbers and Arithmetic:** Review of Number systems, their encoding and basic arithmetic operations, Class of Fixed-Radix Number Systems, Unconventional fixed-point number systems, Representing Signed Numbers, Negative-radix number Systems, Redundant Number Systems, Residue Number Systems.

**Algorithms for Fast Addition:** Basic Addition and Counting, Bit-serial and ripple-carry adders, Addition of a constant: counters, Manchester carry chains and adders, Carry-Look-ahead Adders, Carry determination as prefix computation, Alternative parallel prefix networks, VLSI implementation aspects, Variations in Fast Adders, Simple carry-skip and Carry-select adders, Hybrid adder designs, Optimizations in fast adders, Multi-Operand Addition, Wallace and Dadda trees, Parallel counters, Generalized parallel counters, Adding multiple signed numbers.

**High-Speed Multiplication:** Basic Multiplication Schemes, Shift/add multiplication algorithms, Programmed multiplication, Basic hardware multipliers, Multiplication of signed numbers, Multiplication by constants, Preview of fast multipliers, High-Radix Multipliers, Modified Booth's recoding, Tree and Array Multipliers, Variations in Multipliers, VLSI layout considerations.

**Fast Division and Division Through Multiplication:** Basic Division Schemes, Shift/subtract division algorithms, Programmed division, Restoring hardware dividers, Non-restoring and signed division, Division by constants, Preview of fast dividers, High-Radix Dividers, Variations in Dividers, Combined multiply/divide units, Division by Convergence, Hardware implementation.

**Real Arithmetic:** Representing the Real Numbers, Floating-point arithmetic, The ANSI/IEEE floating-point standard, Exceptions and other features, Floating-point arithmetic operations, Rounding schemes, Logarithmic number systems, Floating-point adders, Barrel-shifter design, Leading-zeros/ones counting, Floating-point multipliers, Floating-point dividers, Arithmetic Errors and Error Control.

**Function Evaluation:** Square-Rooting Methods, The CORDIC Algorithms, Computing algorithms, Exponentiation, Approximating functions, Merged arithmetic, Arithmetic by Table Lookup, Tradeoffs in cost, speed, and accuracy.

**Implementation Topics:** High-Throughput Arithmetic, Low-Power Arithmetic, Fault-Tolerant Arithmetic, Emerging Trends, Impact of Hardware Technology.

### Course Learning Outcomes:

The student will be able to

1. Understand power fundamentals: design objective, quantification of energy and power.
2. Work with fast adders.
3. Analyze the issues related to trade-off between cost, speed and accuracy.
4. Work with high throughput, low power algorithms.

### Recommended Books:

1. *Parhami, B., Computer Arithmetic: Algorithms and Hardware Design, Oxford University Press (2000).*
2. *Koren, I., Computer Arithmetic Algorithms, 2nd Edition, Uni Press (2005) 2<sup>nd</sup> ed.*
3. *Ercegovac, M. and Lang, T., Digital Arithmetic, Elsevier (2005).*

**Evaluation Scheme:**

S.No.	Evaluation Elements	Weightage (%)
1.	MST	30
2.	EST	45
3.	Sessionals (May include Assignments/Projects/Tutorials/Quizes/Lab Evaluations)	25

## PVL218: VLSI Interconnects

<b>L</b>	<b>T</b>	<b>P</b>
<b>3</b>	<b>0</b>	<b>0</b>

**Course Objectives:** In this course the students will learn interconnect models, device models, interconnect analysis and interconnect materials.

**Introduction:** Technology trends, Device and interconnect scaling ,Interconnect Models: RC model and RLC model, Effect of capacitive coupling, Effect of inductive coupling, Transmission line model, Power dissipation, Interconnect reliability.

**Device Models:** Introduction, device I-V characteristics, General format of device Models, device models in explicit expression, device model using a table-Lookup model and effective capacitive model.

**Interconnect analysis:** Time domain analysis: RLC network analysis, RC network analysis and responses in time domain, S domain analysis, circuit reduction via matrix approximation, Analysis using moment matching, transmission lines: step input response.

**Crosstalk analysis:** Introduction, Capacitive coupled and inductive coupled interconnect model and analysis, Transmission line based model.

**Advanced Interconnect materials:** Basic materials: Copper and aluminium. Problem with existing material in deep submicron: Electro-migration effect, surface and grain boundary effect. CNT as an interconnect, impedance parameters of CNT, types of CNT,GNR and Optical interconnects.

### Course Learning Outcomes:

The student will be able to

1. Acquire knowledge about Technology trends, Device and interconnect scaling.
2. Identify basic device and Interconnect Models.
3. Perform RLC based Interconnect analysis.
4. Understand the Problem with existing material in deep submicron.
5. Understand the advanced interconnect materials

### Recommended Books:

1. *Chung-Kang Cheng,John Lillis,Shen Lin and Norman H.Chang, “Interconnect Analysis and Synthesis”,A wiley Interscience Publication(2000).*
2. *Sung-Mo (Steve) Kang, Yusuf Leblebigi, “CMOS Digital integrated circuits analysis and design”, by Tata Mcgraw-Hill, (2007).*
3. *L.O.Chua,C.A.Desoer,and E.S.Kuh, “Linear and Non linear circuits”,McGraw-Hill,1987.*
4. *R.E.Matrick, “Transmission lines for digital and communication networks”, IEEE press,1995.*
5. *Mauricio Marulanda, “Electronic properties of Carbon Nanotubes”, InTech publisher 2011.*

**Evaluation Scheme:**

S.No.	Evaluation Elements	Weightage (%)
1.	MST	30
2.	EST	45
3.	Sessionals (May include Assignments/Projects/Tutorials/Quizes/Lab Evaluations)	25

## PVL333: System on Chip

L T P  
3 0 0

**Course Objectives:** In this course the students will learn SOC design processes, ASIC design flow, EDA tools, architecture design and test optimization with system integration issues.

**Overview of SOC Design Process:** Introduction, Top-down SoC design flow, Metrics of SoC design, Techniques to improve a specific design metric, ASIC Design flow and EDA tools.

**SOC Architecture Design:** Introduction, Front-end chip design, Back-end chip design, Integration platforms and SoC Design, Function Architecture Co-design, Designing Communication Networks, System Level Power Estimation and Modeling, Transaction Level Modeling, Design Space Exploration, Software design in SoCs.

**SOC Design and Test Optimization:** Design methodologies for SoC, Noise and signal integrity analysis, System Integration issues for SoC, SoC Test Scheduling and Test Integration, SoC Test Resource partition.

### Course Learning Outcomes:

The student will be able to

1. Acquire knowledge about Top-down SoC design flow.
2. Understand the ASIC Design flow and EDA tools.
3. Acquire knowledge about Front-end and back-end chip design.
4. Understand the designing communication Networks.
5. Understand the design methodologies for SoC

### Recommended Books:

1. *Wolf, W., Modern VLSI Design: System-on-chip Design, Prentice Hall (2002) 3rd ed.*
2. *Nekoogar, F. and Nekoogar, F., From ASICs to SOCs: A Practical Approach, Prentice Hall (2003).*
3. *Uyemura, J.P., Modern VLSI Design – SOC Design, Prentice Hall (2001).*
4. *Rajsuman, R., System-on-a-chip: Design and Test, Artech House (2000).*
5. *Asheden, P.J. and Mermet J., System-on-Chip Methodologies and Design Languages, Kluwer Academic (2002)*

### Evaluation Scheme:

S.No.	Evaluation Elements	Weightage (%)
1.	MST	30
2.	EST	45
3.	Sessionals (May include Assignments/Projects/Tutorials/Quizzes/Lab Evaluations)	25

## PVL334: High Speed VLSI Design

L T P  
3 0 0

**Course Objectives:** In this course the students will learn the basics of VLSI design for high speed processing, methods for logical efforts, logic styles, latching strategies, interface techniques and related issues.

### Introduction of High Speed VLSI Circuits Design

**Back-End-Of -Line Variability Considerations:** Ideal and non ideal interconnect issues, Dielectric Thickness and Permittivity

**The Method of Logical Effort:** Delay in a logic gate, Multi-stage logic networks, Choosing the best number of stages.

**Deriving the Method of Logical Effort:** Model of a logic, Delay in a logic gate, Minimizing delay along a path, Choosing the length of a path, Using the wrong number of stages, Using the wrong gate size.

**Non-Clocked Logic Styles:** Static CMOS, DCVS Logic, Non-Clocked Pass Gate Families. Clocked Logic Styles: Single-Rail Domino Logic Styles, Dual-Rail Domino Structures, Latched Domino Structures, Clocked Pass Gate Logic.

**Circuit Design Margining:** Process Induced Variations, Design Induced Variations, Application Induced Variations, Noise

**Latching Strategies:** Basic Latch Design, Latching single-ended logic, Latching Differential Logic, Race Free Latches for Pre-charged Logic Asynchronous Latch Techniques

**Interface Techniques:** Signaling Standards, Chip-to-Chip Communication Networks, ESD Protection.

**Clocking Styles:** Clock Jitter, Clock Skew, Clock Generation, Clock Distribution, Asynchronous Clocking Techniques.

### Skew Tolerant Design.

#### Course Learning Outcomes:

The student will be able to

1. Acquire knowledge about High Speed VLSI Circuits Design.
2. Identify the basic Back-End-Of -Line Variability Considerations.
3. Understand the Method of Logical Effort.
4. Understand the Circuit Design Margining and Latching Strategies.
5. Understand the Clocking Styles.

#### *Recommended Books:*



1. *Chung-Kang Cheng, John Lillis, Shen Lin and Norman H. Chang, "Interconnect Analysis and Synthesis", A Wiley Interscience Publication (2000).*
2. *Sung-Mo (Steve) Kang, Yusuf Leblebici, "CMOS Digital integrated circuits analysis and design", by Tata McGraw-Hill, (2007).*
3. *L.O. Chua, C.A. Desoer, and E.S. Kuh, "Linear and Non linear circuits", McGraw-Hill, 1987.*
4. *R.E. Matrick, "Transmission lines for digital and communication networks", IEEE press, 1995.*
5. *Mauricio Marulanda, "Electronic properties of Carbon Nanotubes", InTech publisher 2011.*

**Evaluation Scheme:**

S.No.	Evaluation Elements	Weightage (%)
1.	MST	30
2.	EST	45
3.	Sessionals (May include Assignments/Projects/Tutorials/Quizes/Lab Evaluations)	25

## PVL216: VLSI Subsystem Design

L T P  
3 0 0

**Course Objectives:** In this course the students will learn data processing elements with various architecture design, PLA design concepts, memory design with its clock issues.

**Introduction:** Review of Transistor, Inverter Analysis, CMOS Process and Masking Sequence, Layer Properties and Parasitic Estimation. VLSI Design Flow, Design Methodologies, Abstraction Levels.

**Design of Data Processing Elements:** Adder Architectures, Multiplier Architectures, Counter Architectures, ALU Architectures, Design of Storage Elements: Latches, Flip-Flops, Registers, Register Files.

**Design of Control Part:** Moore and Mealy Machines, PLA Based Implementation, Random Logic Implementation, Micro-programmed Implementation.

**Structuring of Logic Design:** PLA Design, PLA Architectures, Gates Array Cell Design, Concept of Standard Cell Based Design, Cell Library Design.

**Memory Design:** SRAM cell, Various DRAM cells, RAM Architectures, Address Decoding, Read/Write Circuitry, Sense Amplifier and their Design, ROM Design.

**Clocking Issues:** Clocking Strategies, Clock Skew, Clock Distribution and Routing, Clock Buffering, Clock Domains, Gated Clock, Clock Tree. Synchronization Failure and Meta-stability.

### Course Learning Outcomes:

The student will be able to

1. Acquire knowledge to Design of Data Processing Elements.
2. Design of Control Part of digital logic circuit.
3. Acquire knowledge about Structuring of Logic Design.
4. Identify Clocking Issues in digital system design

### Recommended Books:

1. *Weste, N.H.E. and Eshragian, K., Principles of CMOS VLSI Design – A Systems Perspective, Addison Wesley (1994) 3rd ed.*
2. *Rabaey, J.M., Chandrakasan, A., and Nikolic, B., Digital Integrated Circuits - A*
3. *Design Perspective, Pearson Education (2008) 3rd ed.*
4. *Wolf, W., Modern VLSI Design, Prentice Hall (2008) 3rd ed.*
5. *Mead, C. and Conway, L., Introduction to VLSI Systems, B.S. Publisher (1980) 2nd ed.*
6. *Uyemura, J.P., Circuit design for CMOS VLSI, Springer (2005) 2nd ed.*

### Evaluation Scheme:

S.No.	Evaluation Elements	Weightage (%)
1.	MST	30
2.	EST	45
3.	Sessionals (May include	25

	Assignments/Projects/Tutorials/Quizes/Lab Evaluations)	
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## PVL335: Fault Tolerance in VLSI

<b>L</b>	<b>T</b>	<b>P</b>
<b>3</b>	<b>0</b>	<b>0</b>

**Course Objectives:** In this course the students will the basics of fault and error models in VLSI arithmetic, fault tolerance strategies, detection and correction techniques and applications of arithmetic units and systems.

Motivation of fault tolerance in arithmetic systems, Fault and error models in VLSI arithmetic units, Reliability and fault tolerance definitions, Reliability and availability modeling.

Estimation of the reliability and availability of fault tolerant systems, Fault diagnosis, Fault tolerance measurement.

Fault tolerance strategies: detection, correction, localization, reconfiguration, Error recovery, Error detecting and correcting codes.

Detection/correction techniques: modular redundancy, time redundancy (e.g., RESO, RERO, REDWC, RETWV, REXO), datacoding (e.g., AN codes, residue codes, GAN codes, RBR codes, Berger codes, residue number systems), algorithm-based techniques, Reconfiguration techniques.

Applications to arithmetic units and systems (e.g., convolvers, inner product units, FFT units neural networks), Application levels: unit, processing element, subsystem, system. Cost/benefit analysis Fault-tolerant transaction processing systems; Fault-tolerant Networks; Redundant disks (RAID).

Software reliability models, Software fault-tolerance methods: N-version programming, recovery blocks, rollback and recovery.

Architecture and design of fault – tolerant computer systems using protective redundancy.

### Course Learning Outcomes:

The student will be able to

1. Acquire knowledge about fault tolerance in arithmetic circuits.
2. Learn about Fault diagnosis, Fault tolerance measurement.
3. Acquire knowledge about Fault tolerance strategies.
4. Enhance capabilities about applications of fault tolerant designs in arithmetic units and systems.
5. Acquire knowledge on Software reliability models, and methods.

### Recommended Books:

1. *Pradhan, D.K., Fault Tolerant Computer System Design, Prentice Hall (1996).*
2. *Johnson, B.W., Design and Analysis of Fault Tolerant Digital Systems, Addison Wesley (1989).*
3. *Nelson, V.P. and Carroll, B. D., Tutorial: Fault Tolerant Computing, IEEE Computer Society Press (1990)*
4. *Slewiorek, D.P., Swarz, R. S. and Peters A.K., Reliable Computer Systems: Design and Evaluation, A K Peters (1998) 3rd ed.*

### Evaluation Scheme:

S.No.	Evaluation Elements	Weightage (%)
1.	MST	30
2.	EST	45
3.	Sessionals (May include Assignments/Projects/Tutorials/Quizes/Lab Evaluations)	25

## PVL343: Sensor Technology and MEMS

L T P  
3 0 0

**Course Objectives:** In this course the students will learn basic concept of MEMS devices, their working principles, equivalent circuits, different MEMS sensors, fabrication technologies, modeling and characterization tools and calibration techniques.

**Introduction to MEMS:** Introduction to MEMS and Micro sensors, MEMS system-level design methodology, Equivalent Circuit representation of MEMS, Signal Conditioning Circuits.

**Principles of Physical and Chemical Sensors:** Sensor classification, Sensing mechanism of Mechanical, Electrical, Thermal, Magnetic, Optical, Chemical and Biological Sensors.

**Sensor Technology:** Concept of clean room, Vacuum systems, Thin Film Materials and processes (Lithography, oxidation, sputtering, diffusion, CVD, micro machining, Wafer bonding, Wire bonding and Packaging).

**Sensor Modeling:** Numerical modeling techniques, Model equations, different effects on modelling (mechanical, electrical, thermal, magnetic, optical, chemical and biological and example of modelling).

**Sensor characterization and Calibration:** Basic measurement and characterization systems, study of static and dynamic Characteristics, Sensor reliability, Ageing Test, failure mechanism.

**Sensor Applications:** Pressure Sensor with embedded electronics, Accelerometer, RF MEMS Switch with electronics, Bio-MEMS, environmental monitoring (Gas Sensors).

**Future Aspects of MEMS:** NEMS, MOEMS, BIO-MEMS, RF MEMS, OPTICAL MEMS.

### Course Learning Outcomes:

The student will be able to

1. Acquire knowledge about MEMS & Micro Sensors.
2. Understand various micro fabrication technologies.
3. Gather knowledge of characterization tools.
4. Acquire knowledge about Device Applications

### Recommended Books:

1. *Franssila, Sami, Introduction to Microfabrication, John Wiley & Sons, (2010) 2<sup>nd</sup> ed.*
2. *Gad-el-Hak, Mohamed, MEMS: Introduction and Fundamentals, CRC Press (2005) 2<sup>nd</sup> ed.*
3. *Maluf, N., An Introduction to Micro-Electro-Mechanical Systems Engineering, Artech House (2000).*
4. *Ristic, L. (Editor), Sensor Technology and Devices, Artech House (1994).*
5. *Leondes, T.C., MEMS/NEMS Handbook: Techniques and Applications, Springer Press (2007).*
6. *Senturia, S. D., Microsystem Design, Springer (2004).*

### Evaluation Scheme:

S.No.	Evaluation Elements	Weightage (%)
1.	MST	30
2.	EST	45
3.	Sessionals (May include Assignments/Projects/Tutorials/Quizes/Lab Evaluations)	25

## PVL\*\*\*: System Verilog

L T P  
2 0 2

**Course Objectives:** The objective of this course is to provide methods and techniques to verify the functionality of digital electronic systems using System Verilog.

**Data types:** Built-in data types, fixed-size arrays, dynamic arrays, queues, associative arrays, linked lists, array methods, choosing a storage type, creating new types with typedef, creating user-defined structures, type conversion, enumerated types, constants, strings and expression width.

**Procedural statements and routines:** procedural statements, tasks, functions, and void functions, routine arguments, local data storage and time values.

**Connecting the test bench and design:** separating the testbench and design, the interface construct, stimulus timing, interface driving and sampling, top-level scope, program – module interactions, system Verilog assertions and Four-Port ATM router.

**Basic OOP:** Introduction, OOP terminology, creating objects, object deallocation, static variables vs. global variables, class methods, defining methods outside of the class, scoping rules, using one class inside another, understanding dynamic objects, copying objects, public vs. local, straying off course and building a test bench.

**Randomization:** Randomization in System Verilog, Constraint, solution probabilities, controlling multiple constraint blocks, pre\_randomize and post\_randomize functions, random number functions, constraints tips and techniques, common randomization problems, iterative and array constraints, atomic stimulus generation vs. scenario generation, random control, random number generators and random device configuration.

**Threads and interprocess communication:** Threads, disabling threads, interprocess communication, events, semaphores, mailboxes and building a testbench with threads & IPC.

**Laboratory Work:** Modelling and simulation of digital blocks, their verification by using SystemVerilog.

**Course learning outcome (CLO):** The student will be able to:

1. Acquire the knowledge of different data types used in System Verilog.
2. Verify the functionality of design by developing a test bench code.
3. Apply the concepts of object oriented programming in System Verilog.
4. Apply randomization methods in System Verilog.

### **Text Books:**

1. *Chris Spear, System Verilog for Verification A Guide to Learning the Testbench Language Features, Springer, (2008) 2nd Ed.*



2. *Stuart Sutherland, Simon Davidmann and Peter Flake, SystemVerilog for Design Second Edition: A Guide to Using SystemVerilog for Hardware Design and Modeling, Springer (2006); 2nd ed.*

**Reference Book:**

1. *Bhaskar, J., System Verilog Primer, Bsp (2013).*

**Evaluation Scheme:**

S.No.	Evaluation Elements	Weightage (%)
1.	MST	30
2.	EST	45
3.	Sessionals (May include Assignments/Projects/Tutorials/Quizes/Lab Evaluations)	25

## PVL234 Machine Learning

L T P  
3 0 0

**Machine Learning Preliminaries:** Biological vs Machine learning, Learning with a teacher, Learning without a teacher, Connectionist approach to machine learning, Data and patterns, Data visualization, Feature spaces, Pattern spaces, Classification with decision boundaries, Regression, Logistic Regression, Error criteria, Introduction to Python programming, Data types and overview of Machine Learning Libraries.

**Data Preprocessing & Supervised Learning:** Data partitioning into training, test and validation sets, Data scaling and preprocessing, Normalization, Cluster analysis, Dimensionality reduction, Principal Component Analysis (PCA), Linear Discriminant Analysis (LDA), Independent Component Analysis (ICA) for blind signal separation, Naïve Bayes classifier, Decision trees, Random Forest, , K-nearest neighbor classifier.

**Neural Networks Based Learning Machines:** Mc Culloch-Pitts model of a neuron, Solution of XOR-problem, The perceptron convergence theorem, Perceptron as a Bayesian classifier in Gaussian environment, Backpropagation algorithm, Solution of typical classification problems with vanilla neural networks, Radial Basis Function Neural Networks, Support vector Machines (SVMs), Boltzman Machines, Recurrent Neural Networks (RNN).

**Unsupervised and Semi Supervised Learning Algorithms:** K-means clustering, Self-organizing Maps (SOM), Gaussian Mixture Models, Hebbian Learning, Reinforcement learning using Markov Decision Process, Unsupervised Feature Learning using Convolutional Neural Networks (CNN),

**Deep Learning:** Need and scope of Deep Learning, Deep convolutional networks, Deep belief networks, Deep Boltzman Machines, Deep Reinforcement learning, Deep Networks in computer vision, image and video processing, Natural Language Processing (NLP) using deep nets, Auto encoders, LSTM networks for NLP applications, Generalized Adversarial Networks (GANs).

### Course Learning Outcomes (CLOs):

#### The students will be able to:

1. Reconstruct sparse or nearly sparse signals from undersampled data.
2. Solve convex optimization problems for allowing rapid signal recovery and parameter estimation.
3. Apply and compare probabilistic and deterministic approach to compressed sensing.
4. Design adaptive/nonadaptive sampling techniques that condense the information in a compressible signal into a small amount of data.

5. Recover large data matrices from incomplete sets of entries.

**Text Books:**

1. *Probability and Random Processes* by G. Grimmett and D. Stirzaker, 3rd. ed., Oxford University Press
2. *Random Matrices* by M. Mehta, 3rd ed., New York: Academic Press
3. *Numerical Linear Algebra* by LLOYD N. Trefethen and David Bau, III, SIAM
4. *Introductory Lectures on Convex Optimization: A Basic Course* by Y. Nesterov, Kluwer Academic Publisher
5. *Discrete Time Signal Processing* by A. Oppenheim and R. Schaffer, Prentice Hall

**Reference Books:**

1. *Convex Optimization* by S. Boyd and L. Vandenberghe, Cambridge University Press
2. *All of Statistics* by L. Wasserman, Springer

**Evaluation Scheme:**

S.No.	Evaluation Elements	Weightage (%)
1.	MST	30
2.	EST	45
3.	Sessionals (May include Assignments/Projects/Quizzes)	25

## PVL235 RF IC Design

L T P  
3 0 0

**Course Objectives:** The objective of this course is to introduce the theory and concept of RF IC design. Students will also learn to analyze the performance parameters of radio frequency circuits and identify design trade-off of radio frequency communication systems.

**Introduction to RF and wireless technology:** A Wireless World, RF Design Is Challenging and the Big Picture

**Basic concepts in RF design:** General Considerations, Effects of Nonlinearity, Noise, Sensitivity and Dynamic Range, Passive Impedance Transformation, Scattering Parameters and Analysis of Nonlinear Dynamic Systems

**Communication concepts:** Analog Modulation, Digital Modulation, Spectral Regrowth, Mobile RF Communications, Multiple Access Techniques, Wireless Standards

**Transceiver Architectures:** General Considerations, Receiver Architectures, Transmitter Architectures and OOK Transceivers

**Low-noise Amplifiers:** General Considerations, Problem of Input Matching, LNA Topologies, Gain Switching, Band Switching, High-IP2 LNAs and Nonlinearity Calculations

**Mixers:** General Considerations, Passive Down conversion Mixers, Active Down conversion Mixers, Improved Mixer Topologies and Up conversion Mixers

**Passive Devices:** General Considerations, Inductors, Transformers, Transmission Lines, Varactors, Constant Capacitors

**Oscillators:** Performance Parameters, Cross-Coupled Oscillator, Three-Point Oscillators, Voltage-Controlled Oscillators Basic Principles, LC VCOs with Wide Tuning Range, Phase Noise, Design Procedure, LO Interface, Mathematical Model of VCOs and Quadrature Oscillators

**Course Learning Outcomes:** On completion of this course, the students will be able to:

1. Acquire a basic knowledge of RF Circuit design and its challenges
2. Perform calculation related System Design considerations.
3. Design of critical components in CMOS RF IC Design.
4. Design of low-noise Amplifier, Mixer and oscillators

**Recommended Books:**

1. Razavi, B., *RF Microelectronics*, Prentice Hall, Second Edition (2012)
2. Razavi, B., *Design of Analog CMOS Integrated Circuits*, Tata McGraw Hill (2008).

S.No.	Evaluation Elements	Weightage (%)
4.	MST	30
5.	EST	45
6.	Sessionals (May include Assignments/Projects/Tutorials/Quizes/Lab Evaluations)	25

## PEC\*\*\*-OPTOELECTRONICS DEVICES AND CIRCUITS

L T P Cr

3 0 0 3

**Course Objectives:** The main objective of this course is to understand the physics of optoelectronics devices, different types of photon sources and detectors, different modulators- electrooptic and acoustooptic modulators, electroabsorption modulator, basic introduction of holography, fourier optics and holography and fiber optic sensors.

### Course Content Details:

**Review of Semiconductor Electronics:** Overview, Maxwell's Equations and Boundary Conditions, Semiconductor Electronics Equations, Generation and Recombination in Semiconductors, Examples and Applications to Optoelectronic Devices, Semiconductor p-N and n-P Heterojunctions, Semiconductor n-N Heterojunctions and Metal-Semiconductor Junctions.

**Photon Sources and Detectors:** Semiconductor Photon Optical Sources, Light Sources and Transmitters, Light Emitting Diodes, Burrus LEDs, Edge Emitting LEDs, LED Analog Transmission, LED Digital Transmission, Introduction to Laser, Black Body Radiations, Boltzmann Statistics, Einstein Coefficient for Absorption and Emission, Semiconductor Laser Diode, Quantum Well Laser, Cleaved Coupled Cavity ( $C^3$ ) Laser, Index Guide Lasers, Optoelectronics Integrated Circuits-OEICs.

**Electrooptic and Acoustooptic Modulators:** Electrooptic Effects and Amplitude Modulators, Phase Modulator, Kerr Effect and Kerr Modulators, Electrooptic Effects in Waveguide Devices, Scattering of Light by Sound: Raman-Nath and Bragg Diffractions, Coupled-Mode Analysis for Bragg Acoustooptic Wave Coupler.

**Electroabsorption Modulator:** General Formulation for Optical Absorption Due to an Electron-Hole Pair, Franz-Keldysh Effect, Exciton Effect, Quantum Confined Stark Effect (QCSE), Interband Electroabsorption Modulator, Self-Electrooptic Effect Devices (SEEDs).

**Fourier Optics and Holography:** Introduction to Fourier Transform, Image Forming Properties of Lenses, Holographic Optical Element (HOE), HOE Fabrication Materials, Vibration and Motion Analysis by Holographic Techniques, Hologram Interferometry, Stroboscopic Holography, Modulated Beam Holography.

**Fiber Optic Sensors:** Introduction to Sensors, Fiber Optic Sensor in Healthcare, Fiber Optic Sensor Basic, Angiology, Gastroenterology, Oncology, Neurology, Neurology, Fiber Bragg Grating for Strain and Temperature Sensors, High Temperature Borehole, Seismometer with Fiber Optic Displacement Sensors.

### **Course Learning Outcome (CLOs):**

The students will be able to

1. Identify, formulate and solve different optoelectronics devices related problems using efficient technical approaches.
2. Familiarization with the basic physics of optoelectronics devices and interpret various optical parameters of the photonic sources and detectors.
3. Perform the coupled-mode analysis for wave coupler and learn about the different types of effects in electrooptic, electroabsorption and acoustooptic modulators.
4. Realize the concept of new optical technique i.e. fourier optics and identify the most suitable materials for holographic optical element fabrication.
5. Learn the basics of optical sensors and their applications in medical diagnostics for the benefit of public health.

### ***Text Books:***

1. S. C. Gupta, "Optoelectronic Devices and Systems," Second Edition, PHI Learning Private Limited, New Delhi, 2015.
2. Pallab Bhattacharya, "Semiconductor Optoelectronics Devices," Prentice Hall of India Pvt. Ltd., New Delhi, 2006.

### ***Reference Books:***

1. Shun Lien Chuang, "Physics of Optoelectronic Devices," Wiley Series in Pure and Applied Optics, John Wiley & Sons. Inc., 1995.
2. J. Singh, "Opto Electronics-As Introduction to materials and Devices," Mc Graw-Hill International Edition, 1998.

3. B.E.A. Saleh and M.C. Teich, "Fundamental of Photonics, John Wiley and Sons Inc, 2<sup>nd</sup> Edition, 2007.

**Evaluation Scheme:**

S. No.	Evaluation Elements	Weightage (%)
1.	MST	30%
2.	EST	45%
3.	Sessionals (May include Assignments/Projects/Quizes)	25%



**PVL291      SEMINAR      Credit:04**

**Course Learning Outcomes:**

The students will be able to:

1. Identify, formulate, and research literature for complex engineering problems.
2. Use research based methods in analyzing and interpreting data.
3. Make effective oral presentation and prepare a technical report.

**PVL\*\*\*      DESIGN PROJECT      Credit:04**

**Course Learning Outcomes:**

The students will be able to:

1. Formulate, and analyze complex engineering problem to reach logical conclusions.
2. Conduct or simulate experiments by utilizing latest hardware and software tools and apply appropriate techniques for modeling the engineering problem.
3. Present and write technical report with professional ethics.

**PVL493      DISSERTATION      Credit:16**

**Course Learning Outcomes:**

The students will be able to:

1. Design and implementation of identified research problem or industrial projects.
2. Develop acumen for higher education and research.
3. Write technical reports and publish the research work in referred journals, national and international conferences of repute.
4. Foresee how their current and future work will influence/impact the economy, society and the environment.